A multi-charge wireless charging chip

1 Features

- **Supports the latest WPC standard**
  - ✧ Support Qi protocol BPP, EPP certification
- **Working voltage**
  - ✧ 4V ~ 20V
- **Support up to 30W applications**
- **Support 5~15W multiple applications**
  - ✧ 15W+15W
  - ✧ 15W+5W+3W
  - ✧ Power backwards compatible
- **Integrated 2 sets of H-bridge drivers**
  - ✧ One set of 4N H-bridge driver
  - ✧ One set of 2P2N H-bridge driver
- **Integrated internal voltage & current demodulation**
  - ✧ 3-way voltage ASK demodulation
  - ✧ 2-way voltage ASK demodulation
- **Support low-power mode**
- **Support FOD foreign object detection function**
  - ✧ Static FOD detection
  - ✧ Dynamic FOD detection
- **Support external passive crystal oscillator**
- **Support X7R/CBB/NPO capacitors**
- **Support Q value detection**
- **Dynamic power adjustment function (DPM) for USB power supply with insufficient power supply**
- **Input overvoltage, overcurrent, undervoltage, NTC overtemperature protection function**
- **Integrated large-capacity MTP to support repeated firmware upgrades**
- **Support PD3.0, as well as a variety of DP&DM fast charging protocols**
- **Package 6 mm × 6 mm 0.4pitch QFN48**

2 Applications

One-IC Multi-Charger

3 Description

IP6862 is a wireless charging transmitter control SOC IC that supports multi-charging with one core. It integrates 32-bit MCU, ADC, Timer, I2C, H-bridge driver, ASK demodulation & decoding and rich IO resources, and can customize various Qi protocol wireless charging solutions and pass certification tests.

IP6862 integrates various charging head fast charging protocols and supports high voltage wireless fast charging.

IP6862 integrates rich IO resources and supports customization of indicator effects, and users can also customize the indicator through the PC upper computer.

Contents

4 Reversion History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

First edition release (March 2023)

Changes from Revision V1.02 (March 2023) to Revision V1.10 **Page**

- Update Simplify The Application Schematic 4
- Update the legend and description of coil 3 in the Function Description 11
- Update the description of NTC Thermal Protection 12
- Update Typical Application Schematic 16
- Updating the legend for Layout Notes 17
- Update Bom 20

Changes from Revision V1.10 (September 2024) to Revision V1.30 **Page**

- Update power description and add MPP description 1
- Update simplify the application schematic 4
- Update Updating the description of Coil 3 in Function Description 11
- Update the description of NTC Thermal Protection 12
- Updating MPP schematic 16
- Update Bom 20

5 Simplify The Application Schematic

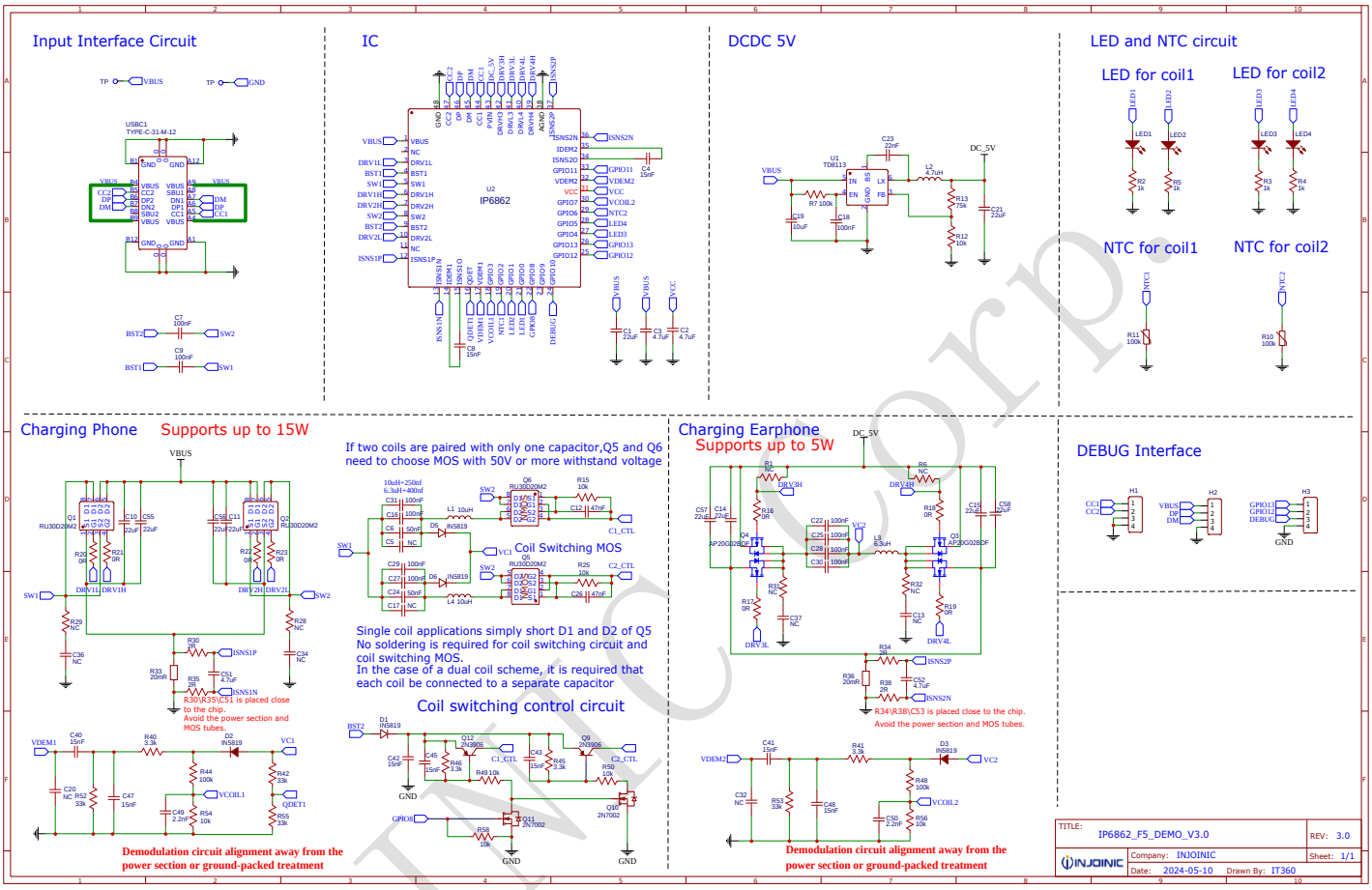


Figure 1 Simplifying The Application Schematic

6 Pin Configuration And Function

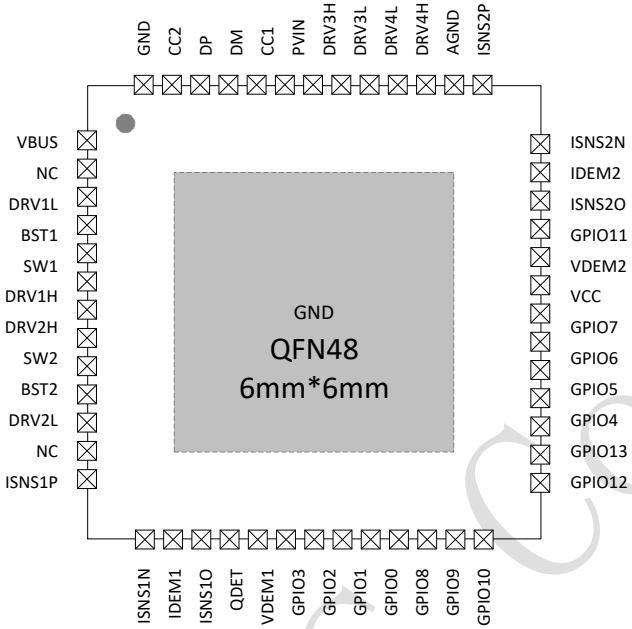


Figure 2 IP6862 Pin Diagram

6.1 Pin Description

Pin No.	Pin Name	Description
1	VBUS	External input voltage
2	NC	NC
3	DRV1L	DRV1 low-side drive
4	BST1	DRV1 bootstraps, Series 47nF capacitors to SW1
5	SW1	DRV1 Half-bridge switch node
6	DRV1H	DRV1 high-side drive
7	DRV2H	DRV2 high-side drive
8	SW2	DRV2 Half-bridge switch node
9	BST2	DRV2 bootstraps, Series 47nF capacitors to SW1
10	DRV2L	DRV2 low-side drive
11	NC	NC
12	ISNS1P	1st set of VBUS current positive sense input
13	ISNS1N	1st set of VBUS current negative sense input
14	IDEM1	ASK demodulate inputs
15	ISNS1O	1st set of sample current amplified output
16	QDET	Q-value detection input

17	VDEM1	ASK demodulate inputs
18	GPIO3	GPIO3
19	GPIO2	GPIO2
20	GPIO1	GPIO1
21	GPIO0	GPIO0
22	GPIO8	GPIO8
23	GPIO9	GPIO9
24	GPIO10	GPIO10
25	GPIO12	GPIO12
26	GPIO13	GPIO13
27	GPIO4	GPIO4
28	GPIO5	GPIO5
29	GPIO6	GPIO6
30	GPIO7	GPIO7
31	VCC	Internal VCC supply, external 4.7uF capacitor to GND
32	VDEM2	ASK demodulate inputs
33	GPIO11	GND
34	ISNS2O	2^{nd} set of sample current amplified output
35	IDEM2	ASK demodulate inputs
36	ISNS2N	2^{nd} set of VBUS current positive sense input
37	ISNS2P	2^{nd} set of VBUS current negative sense input
38	AGND	Analog GND
39	DRV4H	DRV4 high-side drive
40	DRV4L	DRV4 low-side drive
41	DRV3L	DRV3 high-side drive
42	DRV3H	DRV3 low-side drive
43	PVIN	Input voltage V_{IN}
44	CC1	Type_C detect pin CC1
45	DM	USB DM
46	DP	USB DP
47	CC2	Type_C detect pin CC2
48	GND	GND

7 Functional Block Diagram

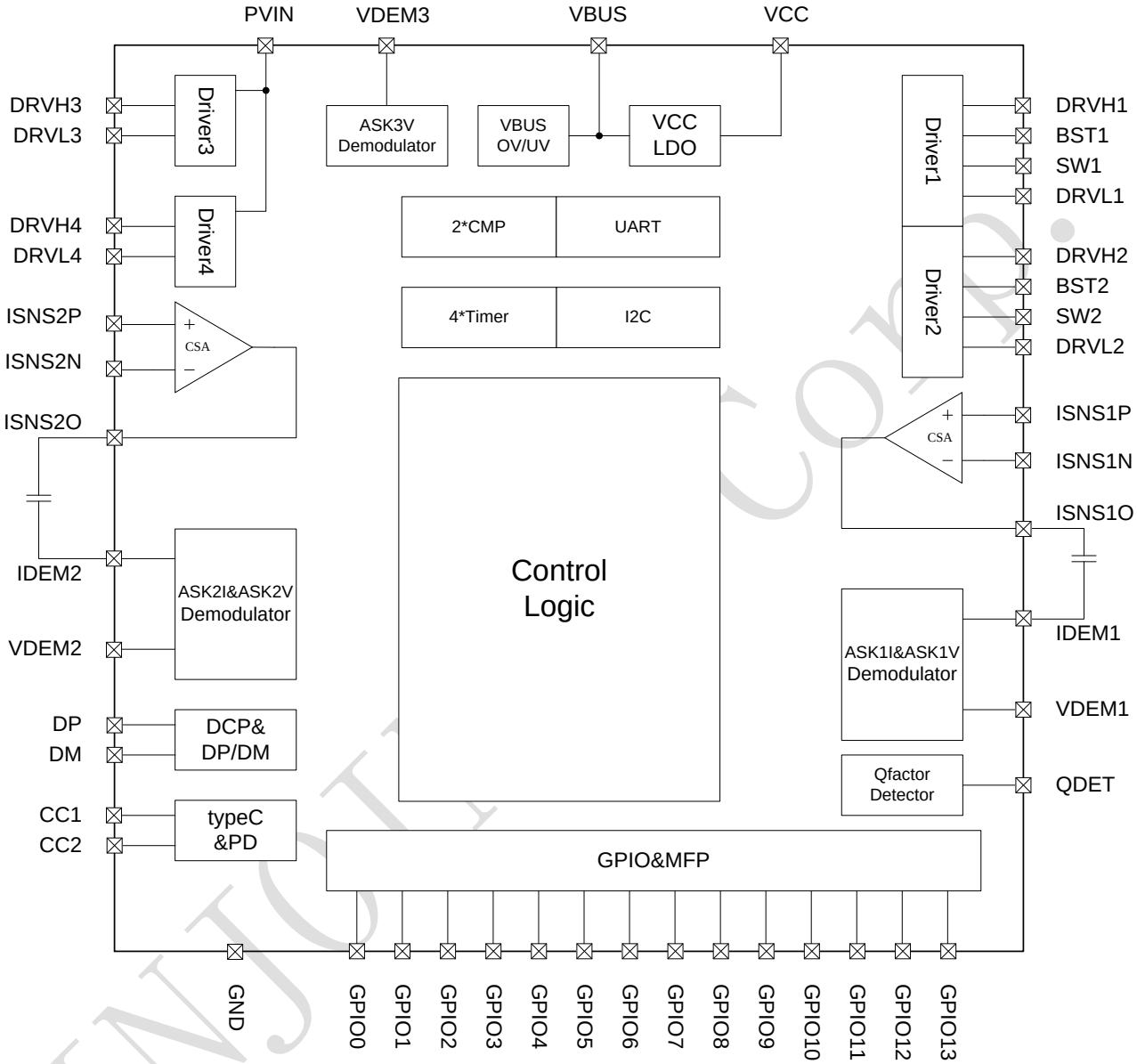


Figure 3 Functional Block Diagram

8 Absolute Maximum Ratings

Parameters	Symbol	Min	Max	Unit
Input Voltage Range	VIN	-0.3	26	V
	CC1, CC2	-0.3	12	
	DP, DM	-0.3	8	
Junction Temperature Range	T_J	-40	125	℃
Storage Temperature Range	T_{stg}	-60	125	℃
Package Thermal Resistance（JunctionTemperature to environment）	θ_{JA}	40		℃/W
Human Body Model (HBM)	ESD	4		KV

* Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to Absolute Maximum Rated conditions for extended periods may affect device reliability.

9 Recommended Operating Conditions

Parameters	Symbol	Min	Typ	Max	Unit
Input Voltage Range	V_{IN}	4.0	5/9/12	21.5	V
I/O Voltage Range	IO0~IO15	GND-0.3		V_{CC}+0.3	V
	DP, DM,CC1,CC2	GND-0.3		5.5	

*Devices' performance cannot be guaranteed when working beyond those Recommended Operating Conditions.

10 Electrical Characteristics

Unless otherwise specified, TA =25℃

Parameters	Symbol	Test Condition	Min	Typ	Max	Unit
Input Voltage	V_{IN}		4.0	5/9/12	21.5	V
Internal power supply	V_{CC}		3.0	3.6	5	V
Input high level	V_{IH}		0.7*V_{CC}			V
Input low level	V_{IL}				0.3*V_{CC}	V
Input high level	V_{OH}			V_{CC}		V
Input low level	V_{OL}			GND		V
LED Output current capability	Source current（LED1、LED2）	Source current to output high level is 0.8*VCC		2	4	mA

11 Function Description

11.1 Fast Charge Input Request

Built-in PD protocol input request module, apply fast charging voltage to PD adapter through CC1, CC2.

Built-in DP&DM input fast charging protocol request module, apply fast charging voltage to the adapter through DP&DM.

11.2 Full Bridge Drive and Digital Demodulation

11.2.1 Coil 1

The IP6862 has a built-in 4N full-bridge driver, and the peripheral circuit needs to build a full-bridge 4xNMOS to implement the wireless charging controller.

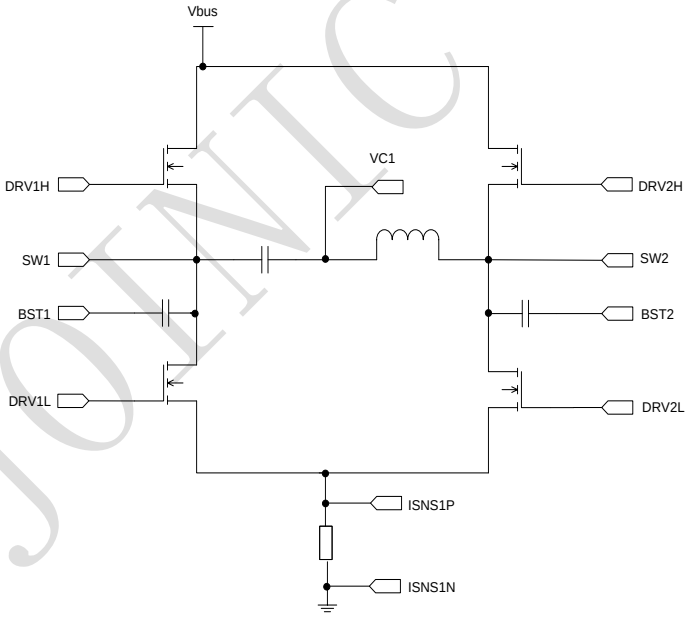


Figure 4 4xNMOS Full-Bridge Driver Application Circuit

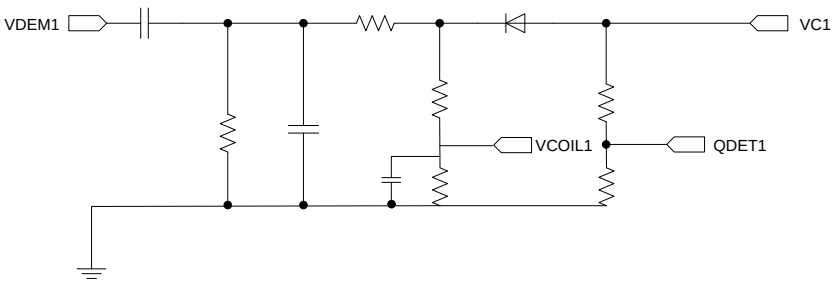


Figure 5 4xNMOS Voltage Decoder Circuit

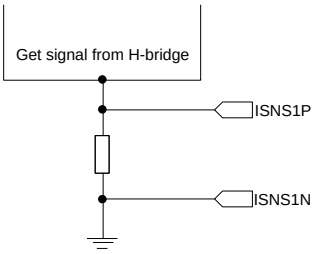


Figure 6 4xNMOS Current Decoder Circuit

11.2.2 Coil 2

The IP6862 has a built-in 2P2N full-bridge driver, and the peripheral circuit needs to build two full-bridge P+NMOS to implement the wireless charging controller.

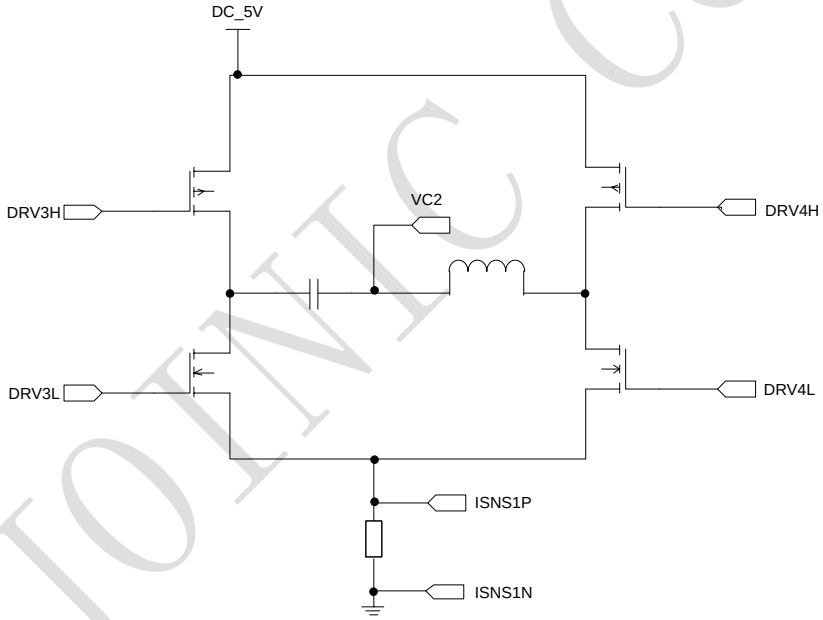


Figure 7 2P2NMOS Full-Bridge Driver Application Circuit

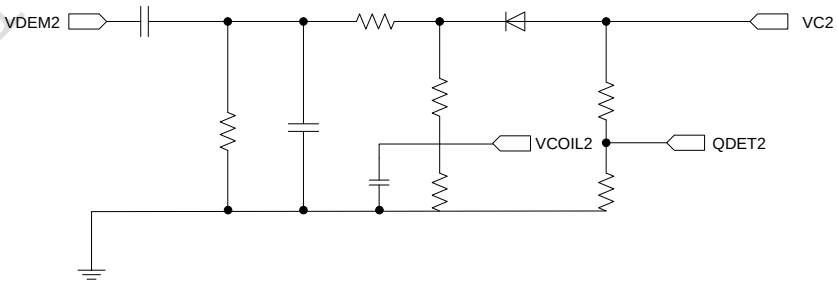


Figure 8 2P2NMOS Voltage Decoder Circuit

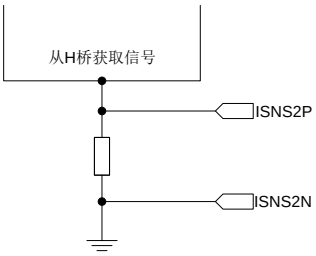


Figure 9 2P2NMOS Current Decoder Circuit

11.2.3 Coil 3

The IP6862 has a built-in 2P2N full-bridge driver, and the peripheral circuit needs to build two full-bridge P+NMOS to implement the wireless charging controller

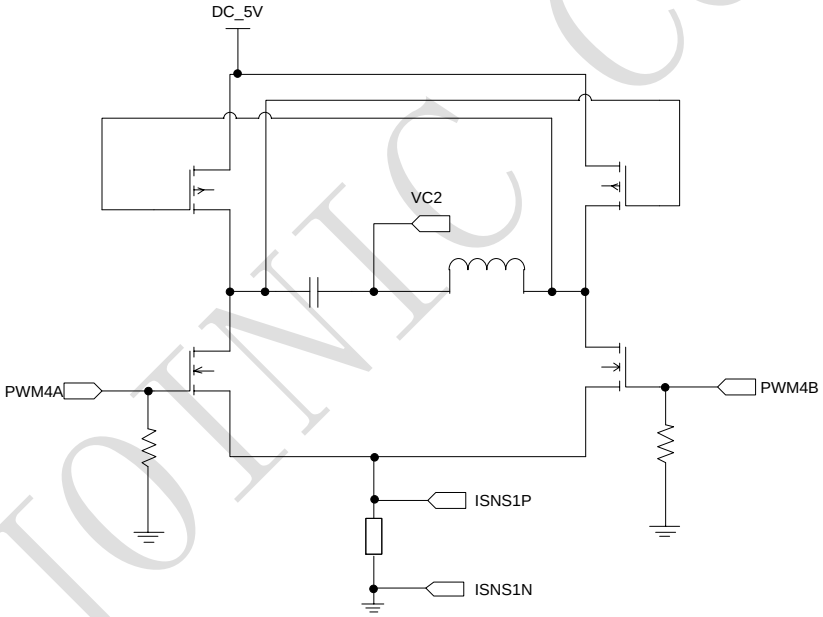


Figure 10 2P2NMOS Full-Bridge Driver Application Circuit

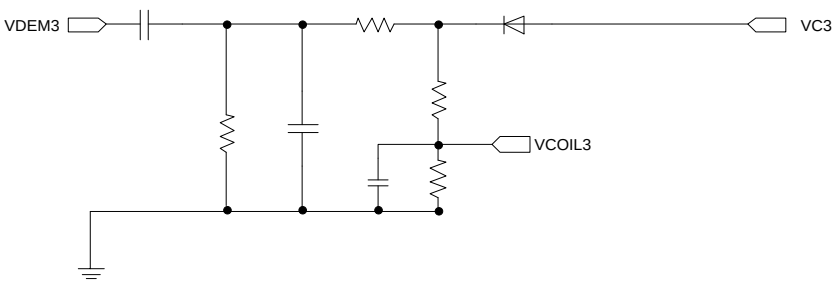


Figure 11 2P2NMOS Current Decoder Circuit

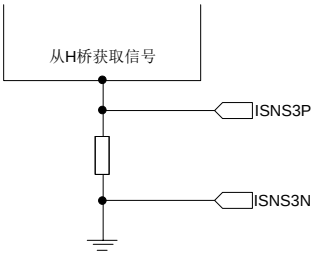


Figure 12　2P2NMOS Current Decoder Circuit

11.3 DPM

For USB power supply with insufficient power supply capacity, it has dynamic power management function to keep the charging state uninterrupted. When the system detects that the input voltage is below 4.3V, the DPM function is activated to reduce the transmit power and hold it. When the input voltage returns to above 4.75V and the input current is reduced by 200mA compared to when it entered DPM, the system exits the DPM state.

11.4 FOD Parameter Adjustment

IP6862 supports static FOD foreign object detection and dynamic FOD foreign object detection.

Static FOD means that foreign objects on the coil can be detected when there is no wireless charging.

Dynamic FOD means being in the process of wireless charging and being able to detect foreign objects on the coil.

IP6862 can detect the Q value before entering charging to determine whether foreign objects exist, and can use the power loss method to determine whether foreign objects are present after entering charging.

11.5 NTC Thermal Protection

The NTC of IP6862 calculates the temperature in the following way:

The NTC pin outputs a fixed current of 20μA, and the NTC PIN determines the NTC temperature by sampling the voltage at the NTC pin; this shutdown feature is to provide enhanced applications and is not limited to thermal shutdown. When the voltage of NTC pin is less than 0.5V, the system will enter NTC protection and end power transfer; after entering NTC protection, the NTC pin voltage is greater than 0.72V and normal charging resumes; if NTC application is not used, the pin is grounded through 100K resistor.

1.Refer to the NTC resistor data sheet to find the resistance - temperature relationship table

2.According to the protection temperature point, find the corresponding resistance value R_NTC

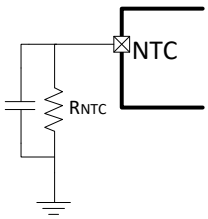


Figure 13 NTC Detection Circuit

Thermistor Recommended Parameters:R_{NTC}=100K@25℃ B=3950；

11.6 Efficiency Curve Test

Using IDT P9221 solution for RX device, the relationship of efficiency and system output power

$$\eta_{\text{system}} = \frac{P_{\text{OL}}}{P_{\text{in}}}$$

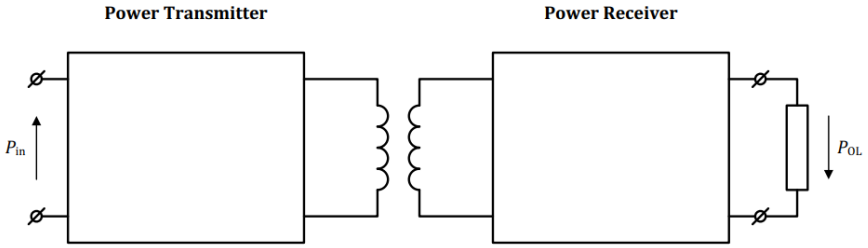


Figure 14 Wireless Charging Power Conversion Model

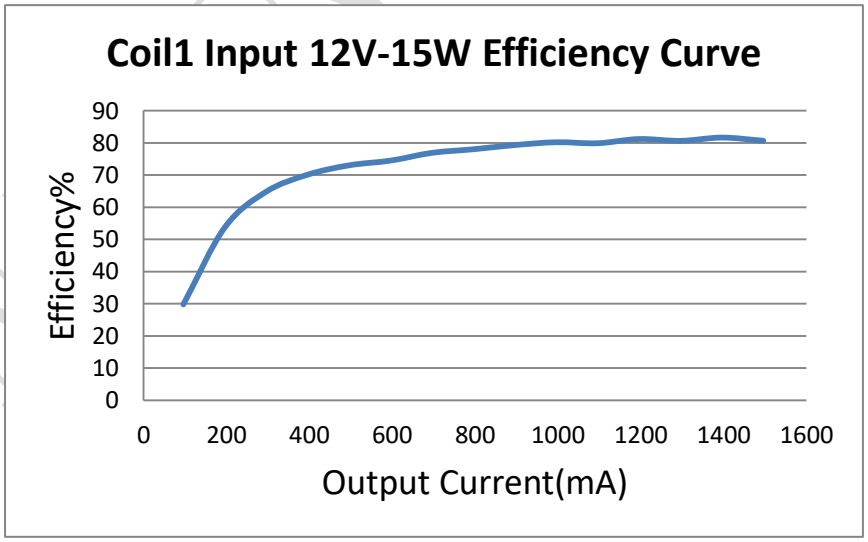


Figure 15 Coil 1 Loaded 15W Efficiency (Use IDT P9221_R RX)

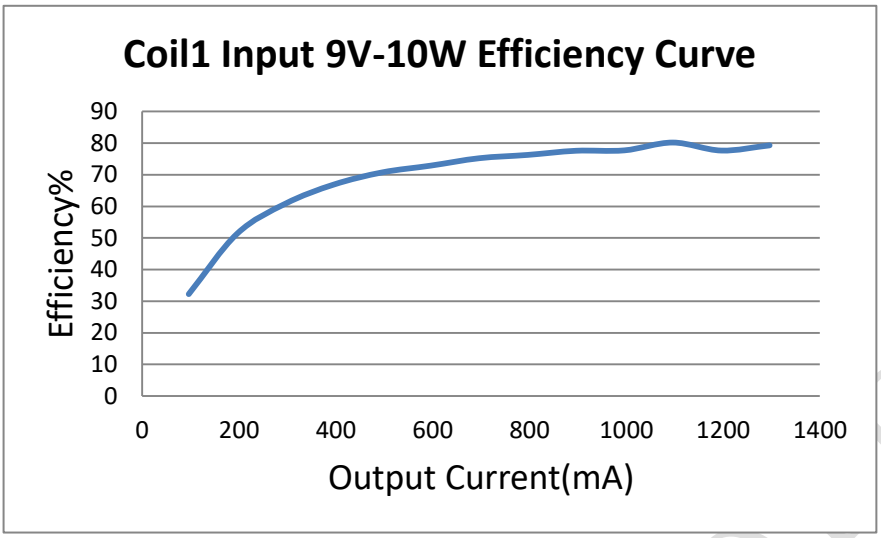


Figure 16 Coil 1 Loaded 10W Efficiency (Use IDT P9221_R RX)

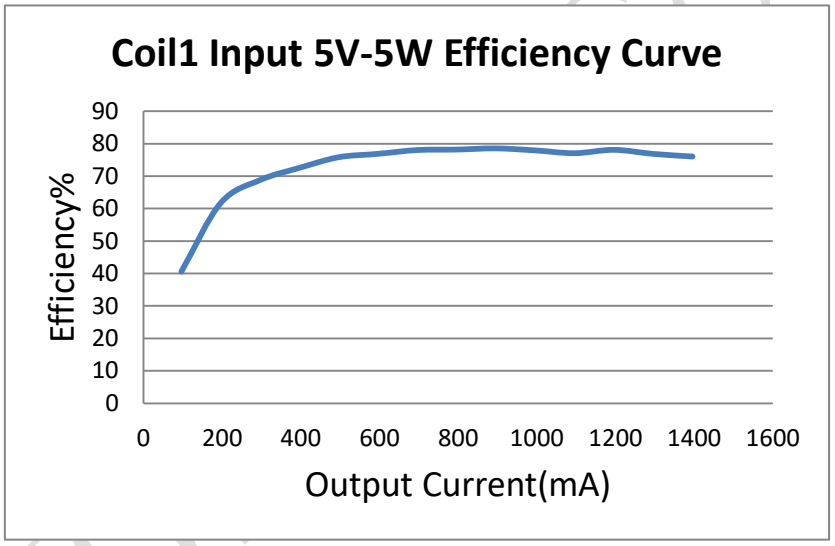


Figure 17 Coil 1 Loaded 5W Efficiency (Use IDT P9221_R RX)

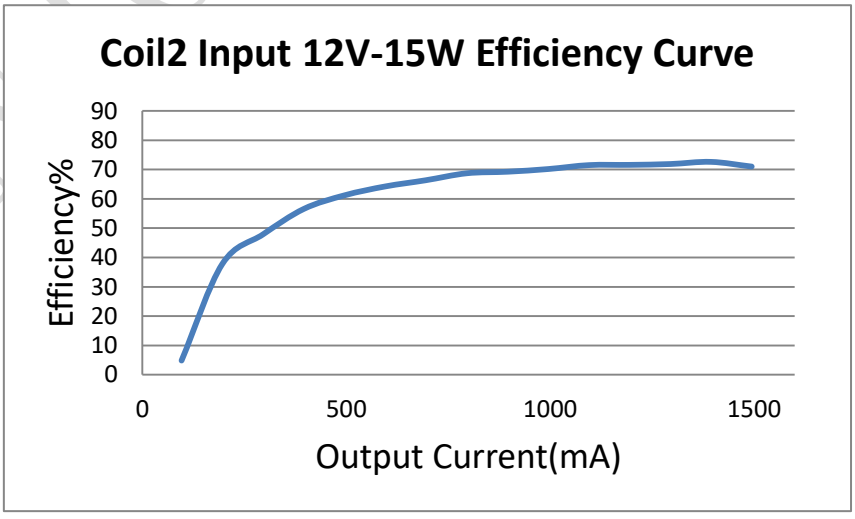


Figure 18 Coil 2 Loaded 15W Efficiency (Use IDT P9221_R RX)

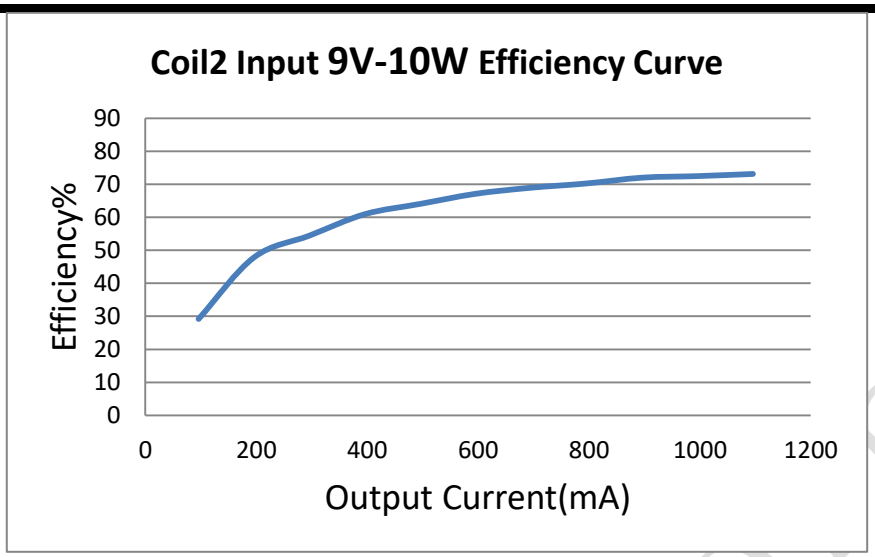


Figure 19 Coil 2 Loaded 10W Efficiency (Use IDT P9221_R RX)

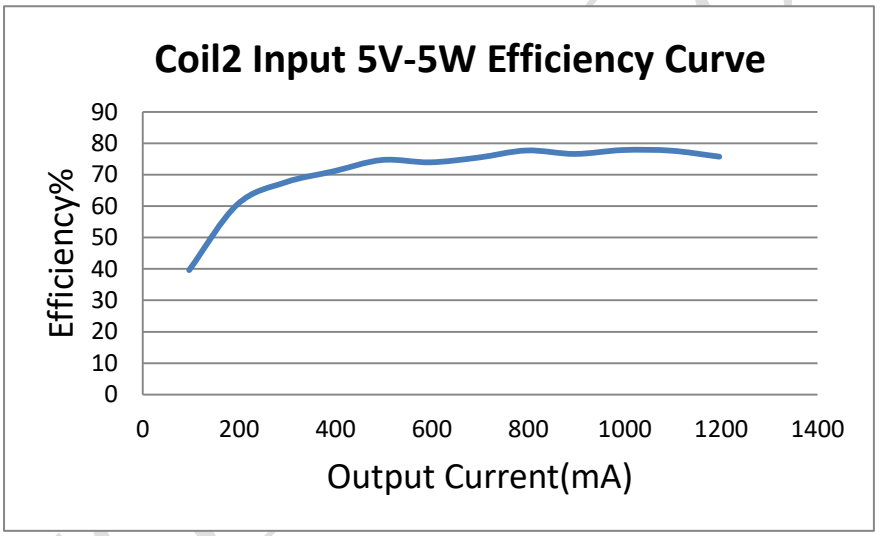


Figure 20 Coil 2 Loaded 5W Efficiency (Use IDT P9221_R RX)

12 Application Notes

IP6862 can be used with different transmitting coils and resonant capacitors to realize different power wireless charging solutions.

13 Firmware Upgrade Instructions

IP6862 can repeatedly upgrade the firmware and needs to be upgraded by using the supporting upgrade tool.

14 Typical Application Schematic

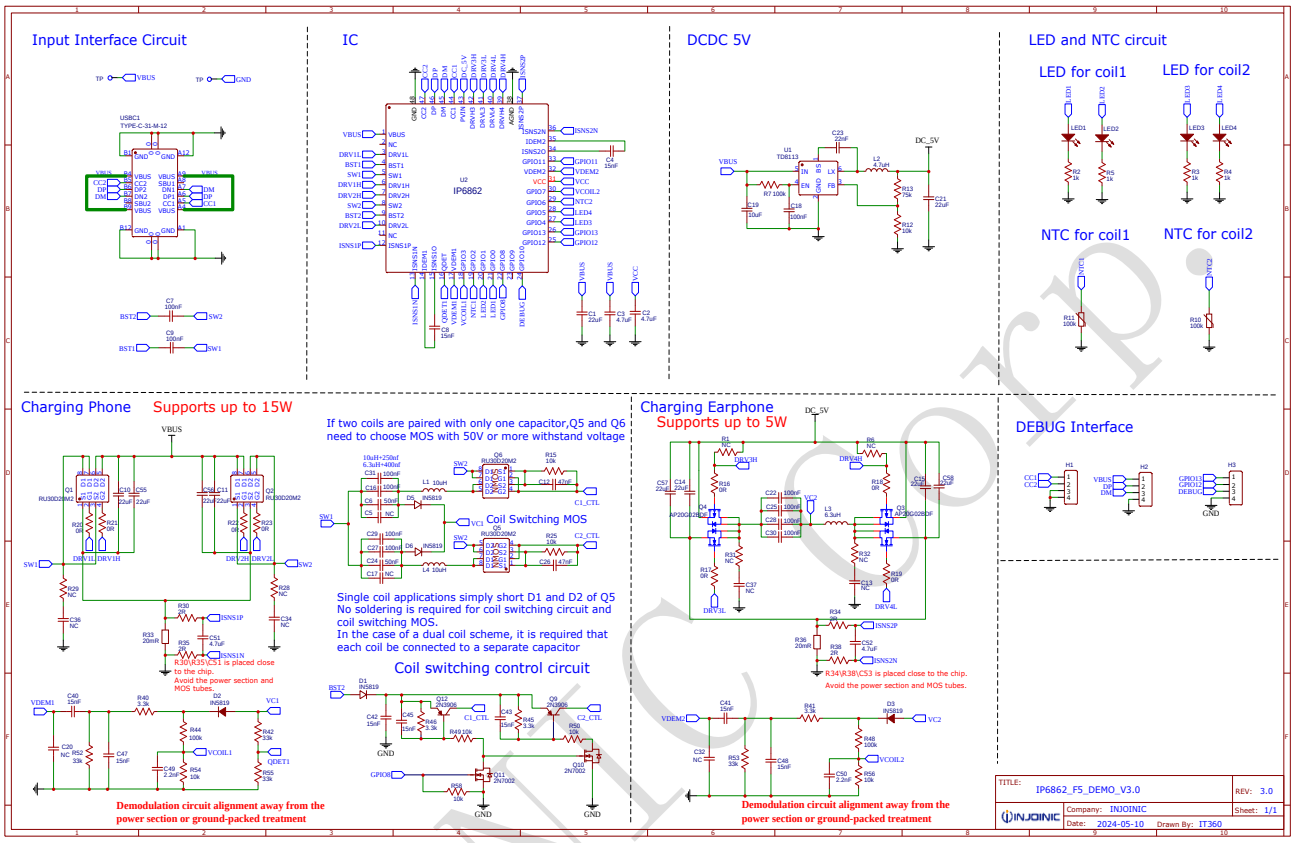


Figure 21 Typical Application Schematic

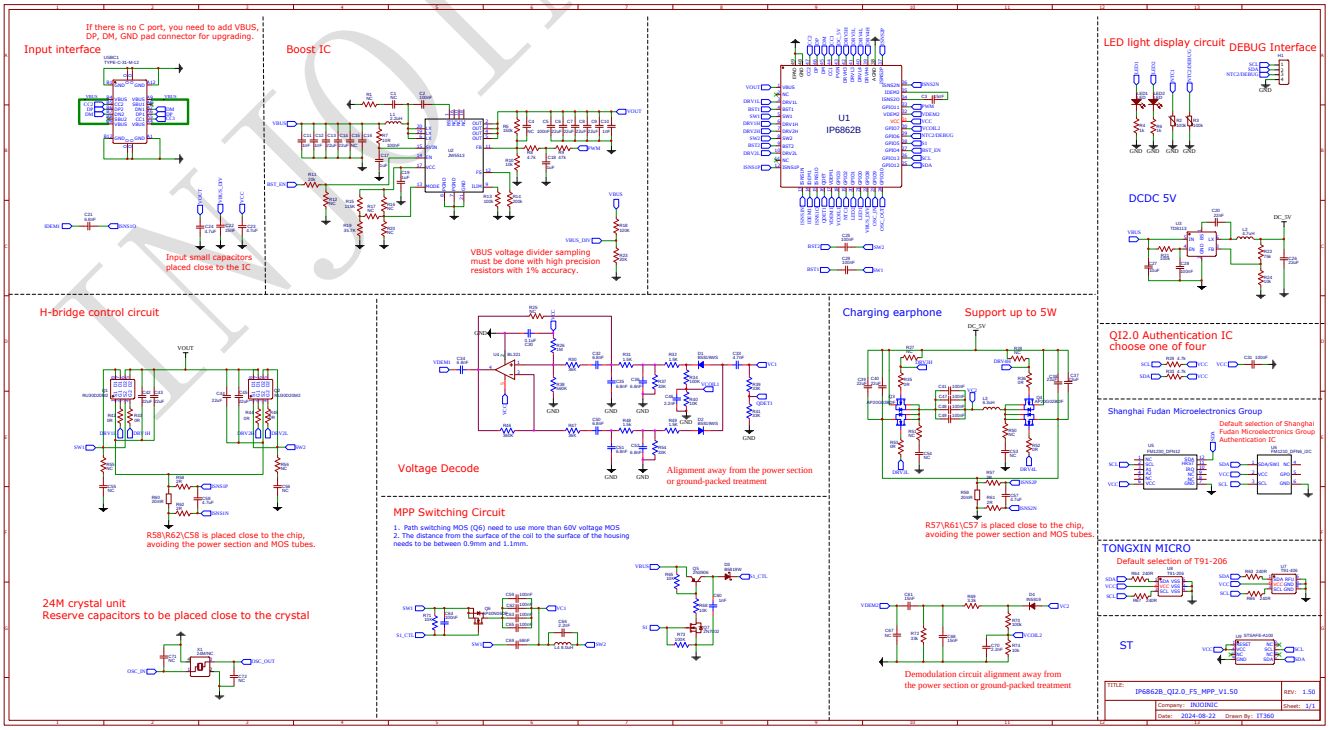
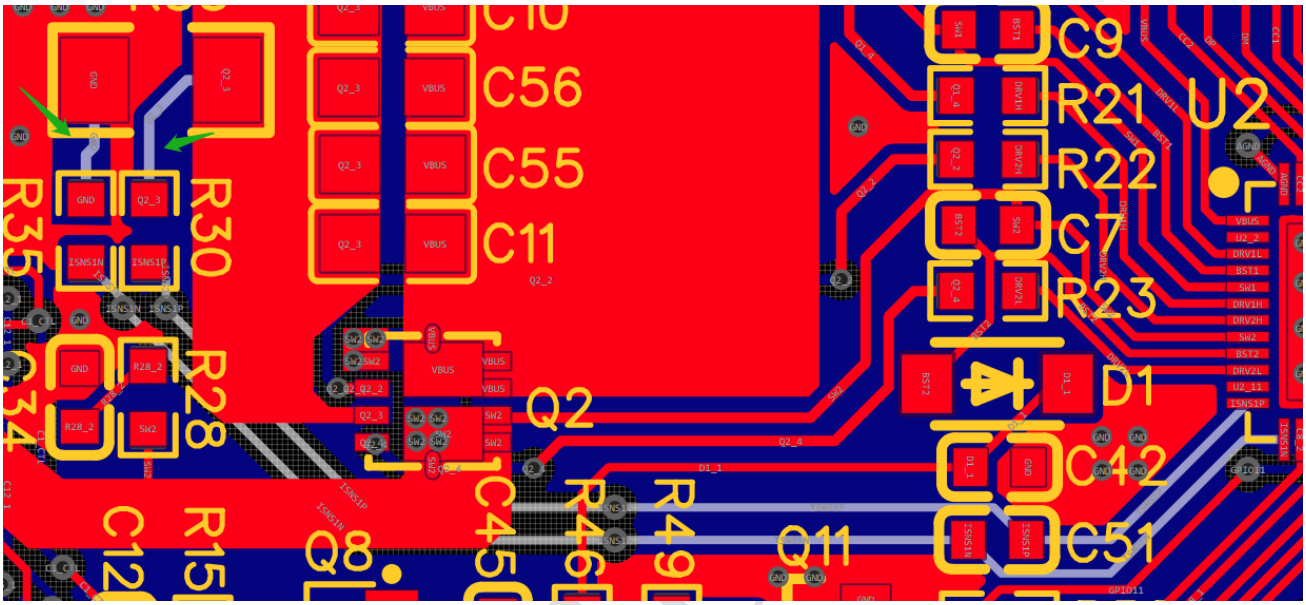


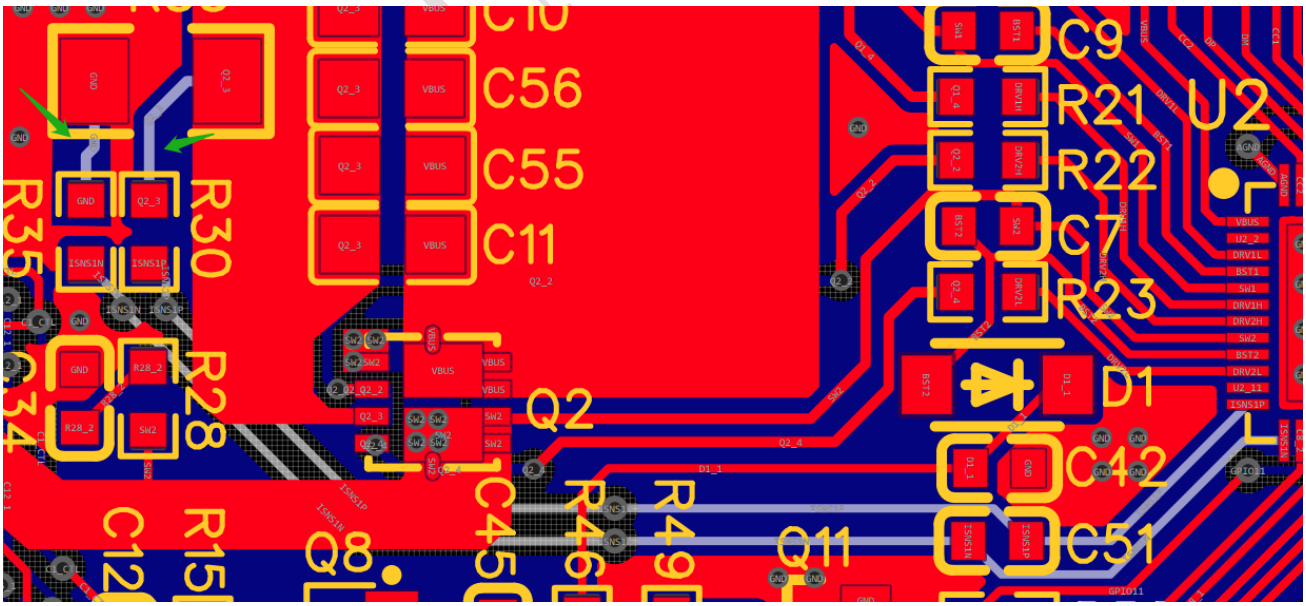
Figure 22 MPP Certification Schematic

15 Layout Notes

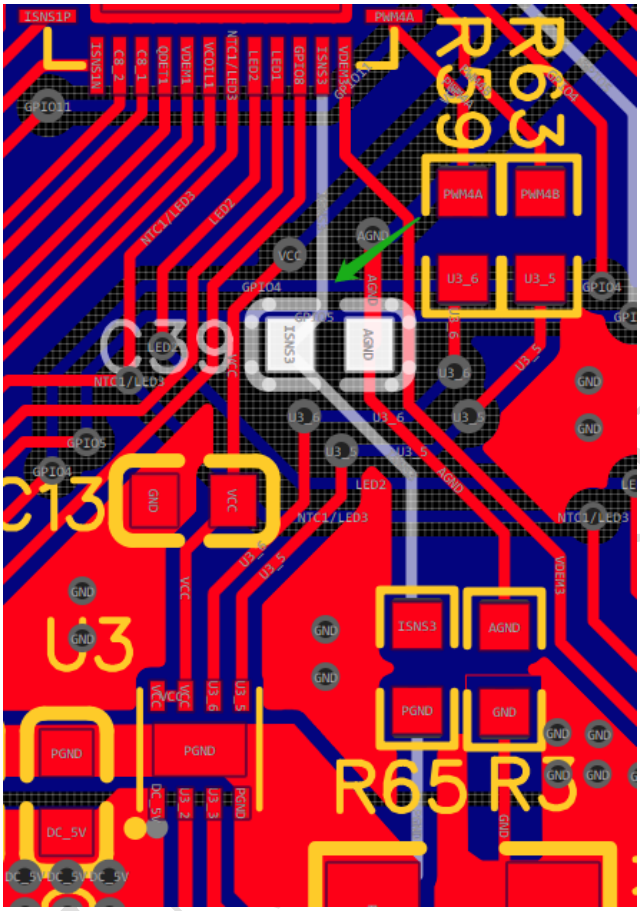
As shown in the figure below: the positive pole and negative pole of the 20mR Jepsun Sampling resistor of coil 1 need to be individually defferential pair to the IC's ISNS1P and ISNS1N; and the routing of GND needs to be separated from the copper laying of GND, there can be no overlap.



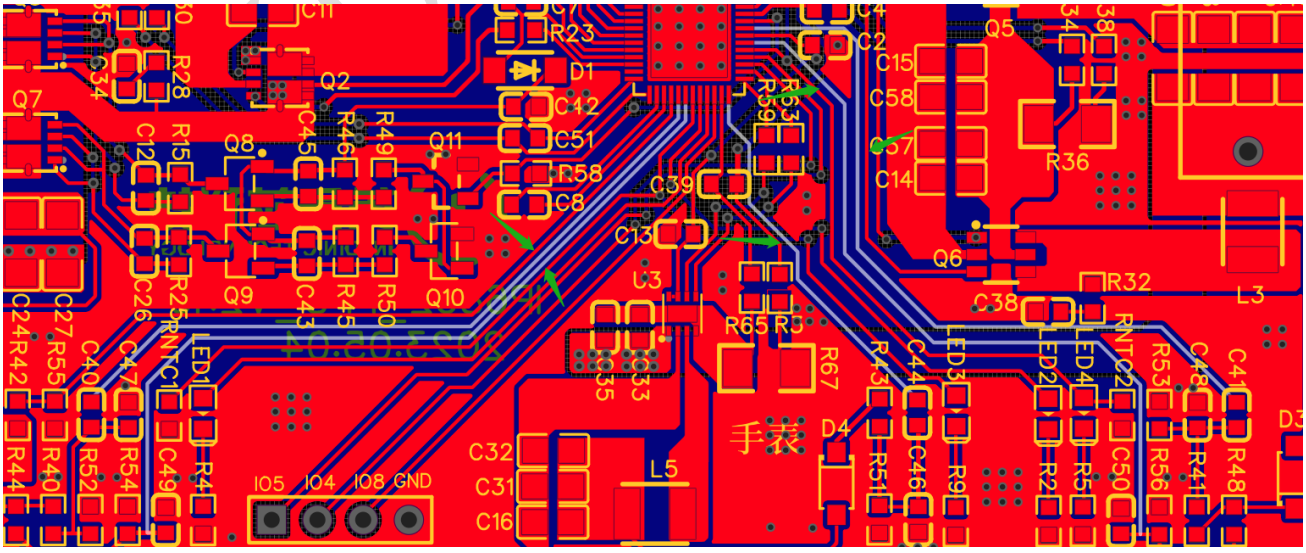
As shown in the figure below: the positive pole and negative pole of the 20mR Jepsun Sampling resistor of coil 2 need to be individually defferential pair to the IC's ISNS2P and ISNS2N; and the routing of GND needs to be separated from the copper laying of GND, there can be no overlap.



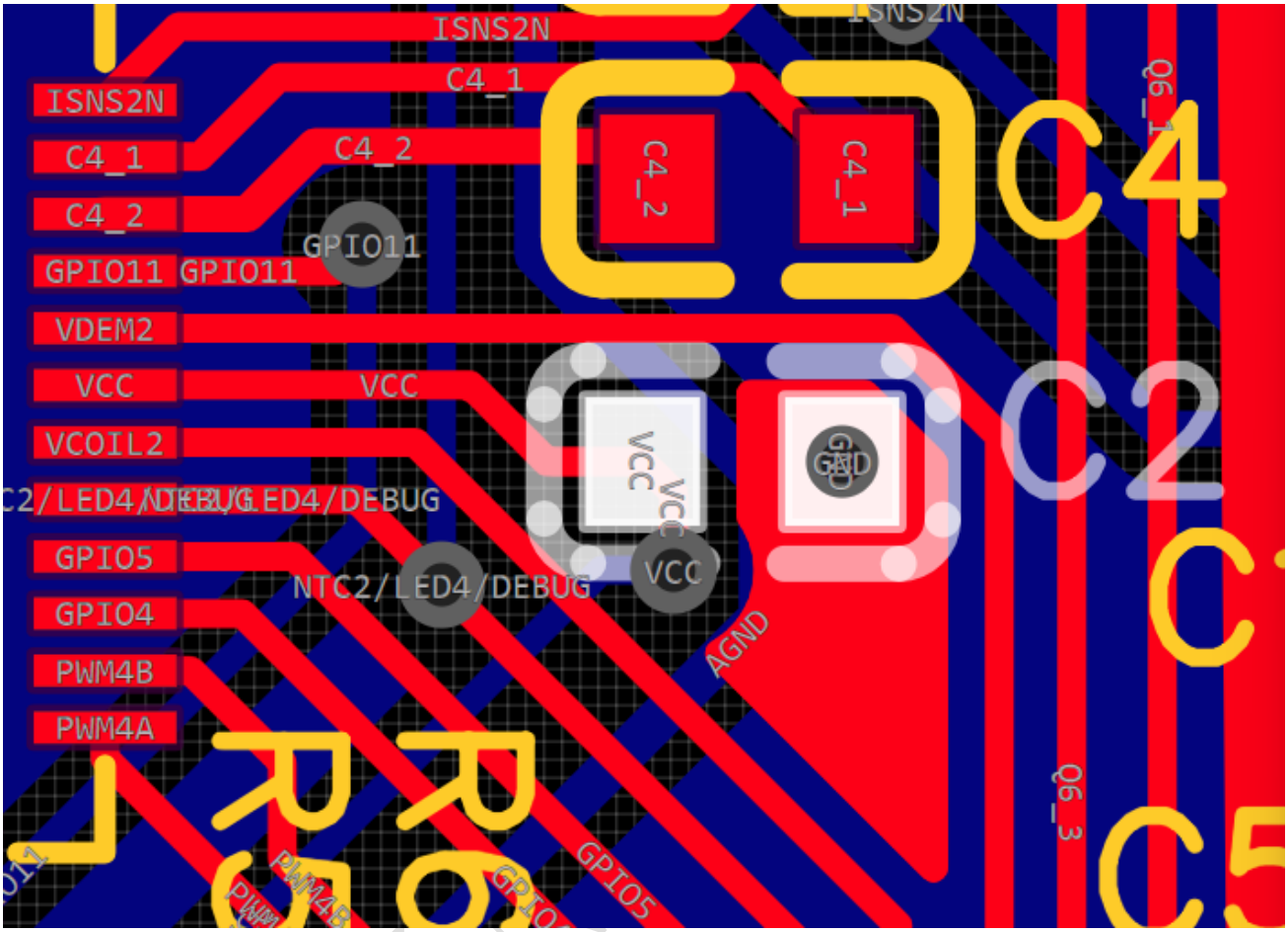
As shown in the figure below: the upper end of the 20mR Jepsun Sampling resistor of coil 3 needs to be wired separately, and the filter capacitor needs to be placed close to the chip pin.



As shown in the figure below: the VCOIL and VDEM routing of the IP6862, as far away from resonant capacitors, coils and other power routing as possible.



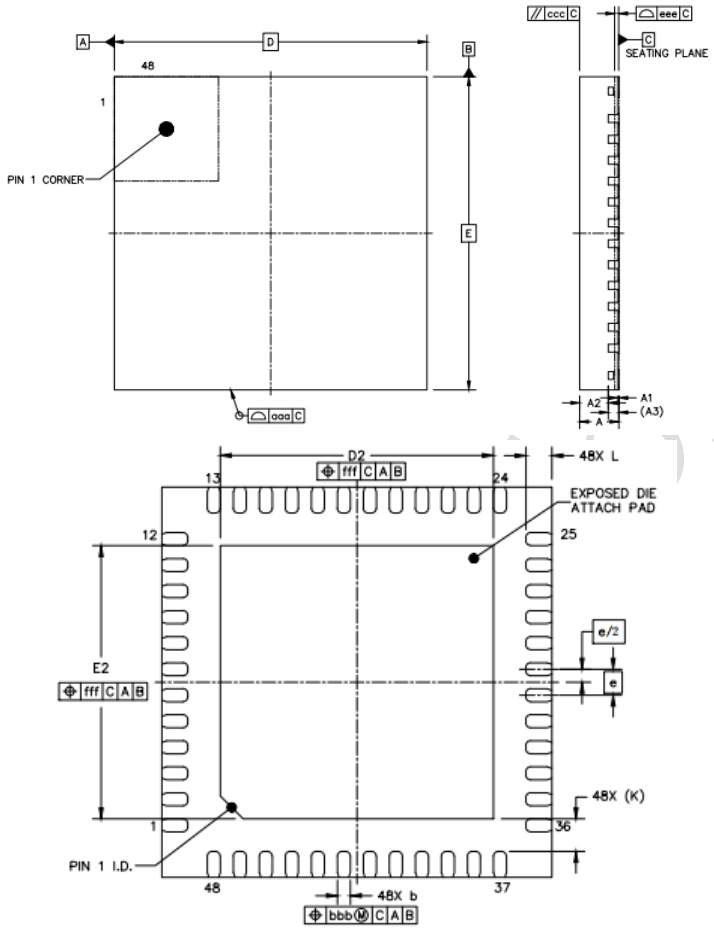
As shown in the figure below, the VCC capacitor of IP6862 needs to be placed close to the IC pin.



16 BOM

Item	Part Name	Description&Specification	Description	Qty	Note
1	4.7uF	C0603	C2,C3,C51,C52	4	
2	22nF	C0603	C23	1	
3	15nF	C0603	C4,C8,C40,C41,C42,C43,C45,C47,C48	9	
4	22uF	C0805	C1,C10,C11,C14,C15,C21,C55,C56,C57,C58	10	
5	10uF	C0603	C18,C19	2	
6	100nF	C0603	C7,C9	2	
7	47nF	C0603	C12,C26	2	
8	100nF	C1206	C17,C24,C27,C29,C22,C25,C28,C30	8	
9	2.2nF	C0603	C49,C50	2	
10	IN5819	SOD-123F	D1,D2,D3,D5,D6	5	
11	4.7uH	IND-SMD	L2	1	
12	6.3uH	A11 线圈	L3,L4	2	
13	LED	LED0603_RED	LED1,LED2,LED3,LED4	4	
14	RU30D20M2	PDFN3333-8	Q1,Q2,Q5,Q6	4	
15	AP20G02BDF	DFN-8	Q3,Q4	2	
16	2N3906	SOT-23-3	Q9,Q12	2	
17	2N7002	SOT-23-3	Q10,Q11	2	
18	100k	R0603	R7,R10,R11,R44,R48	5	
19	1k	R0603	R2,R3,R4,R5	4	
20	0R	R0603	R16,R17,R18,R19,R20,R21,R22,R23	8	
21	75k	R0603	R13	1	
22	10k	R0603	R12,R15,R25,R49,R50,R54,R56,R58	8	
23	2R	R0603	R30,R34,R35,R38	4	
24	20mR	R1206	R33,R36	2	
25	3.3k	R0603	R40,R41,R45,R46	4	
26	33k	R0603	R42,R52,R53,R55	4	
27	TD8113	SOT-23-6	U1	1	
28	IP6862	IP6862_QFN48_6*6	U2	1	
29	TYPE-C-31-M-12	USB-C_SMD	USBC1	1	

17 Package



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.7	0.75	0.8
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	---	0.55	---
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.15	0.2	0.25
BODY SIZE	X	D		6 BSC	
	Y	E		6 BSC	
LEAD PITCH		e		0.4 BSC	
EP SIZE	X	D2	4.1	4.2	4.3
	Y	E2	4.1	4.2	4.3
LEAD LENGTH		L	0.3	0.4	0.5
LEAD TIP TO EXPOSED PAD EDGE		K		0.5 REF	
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		ccc		0.1	
COPLANARITY		eee		0.08	
LEAD OFFSET		bbb		0.07	
EXPOSED PAD OFFSET		fff		0.1	

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