

## 10W Wireless Power Receiving Chip

### 1 Features

- **High-integration wireless power receiving SOC**
  - ◇ Built-in 32-bit MCU
  - ◇ Built-in 10k Bytes MTP, 1k Bytes RAM
  - ◇ Built-in multi-channel 12bit SAR ADC
- **Support 10W wireless power reception**
  - ◇ Built-in high-efficiency full-bridge synchronous rectifier circuit
  - ◇ Built-in wireless charging overvoltage protection circuit
  - ◇ Built-in ASK modulation circuit
  - ◇ Built-in FSK demodulation circuit, support private protocol
  - ◇ Support the latest protocol standard of WPC Qi
- **Built-in voltage regulator LDO**
  - ◇ Output voltage gear 3.6 ~ 9V programmable
  - ◇ Output current up to 1.6A
  - ◇ Undervoltage protection, overcurrent protection
- **Anti-offset ability**
  - ◇ LDO Input Dynamic Power Management (DPM)
  - ◇ LDO output current dynamic limit (Current Limit)
- **Multiple power supply methods**
  - ◇ Wireless power supply, VRECT pin input
  - ◇ Wired power supply, VBUS pin input
  - ◇ Support wired charging and wireless charging path switching
- **Reliable over temperature, over voltage and over current protection circuit**
- **Power consumption is less than 2uA in deep sleep mode**
- **4mm\*4mm 0.5 pith QFN24 package**

### 2 Applications

- Wireless power receiving device
- Wireless charging mobile juicing cup
- Wireless charging mobile fruit and vegetable washing machine

### 3 Description

IP6832 is a highly integrated wireless charging receiver SOC that supports the WPC Qi standard. The chip integrates a high-efficiency full-bridge synchronous rectification circuit to realize AC-DC conversion. The rectified output voltage, VRECT, is regulated by the internal LDO and outputs a stable DC voltage for subsequent loads.

IP6832 built-in 32-bit MCU and rich peripheral resources, so external MCU can be omitted during product development.

IP6832 uses QFN24 (4mm\*4mm) package, with peripheral streamlined application circuit, which greatly saves PCB footprint and can be easily integrated into products with compact space.

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## 4 Reversion History

Note: Page numbers of previous editions may differ from those of the current edition.

<b>Version V1.00 changed in March 2023</b>	<b>Page</b>
• First Release.....	1
<b>Version V1.10 changed in July 2023</b>	<b>Page</b>
• Add VRECT Overvoltage Protection Circuit.....	12
<b>Version V1.20 changed in May 2024</b>	<b>Page</b>
• Update Typical Application Schematic.....	12
• Add VRECT Overvoltage Protection Circuit.....	12

## 5 Application Diagram

### 5.1 Wireless Power Receiving Application

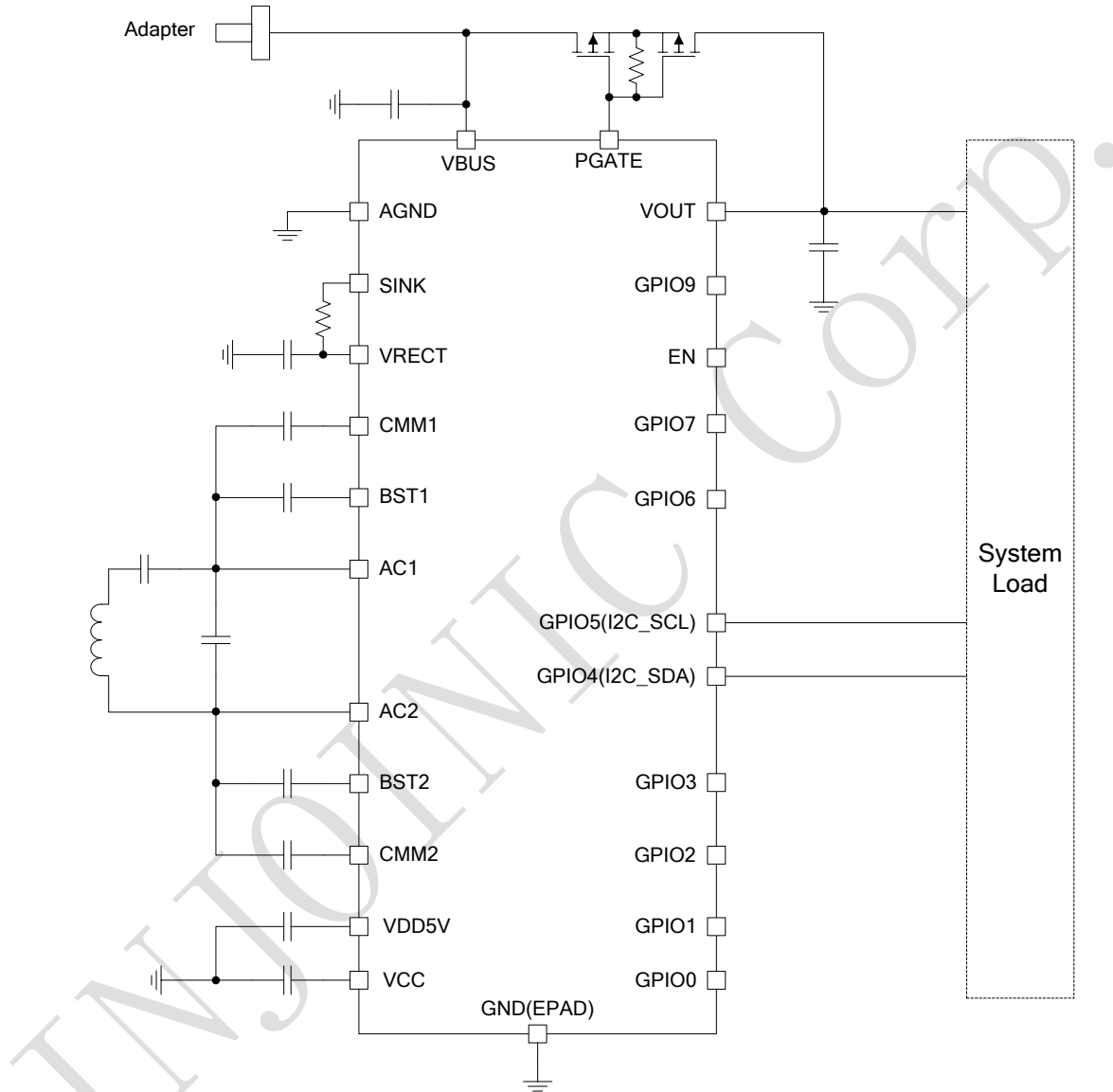


Figure 1 IP6832 Wireless Power Receiving Application

## 6 Pin Definition

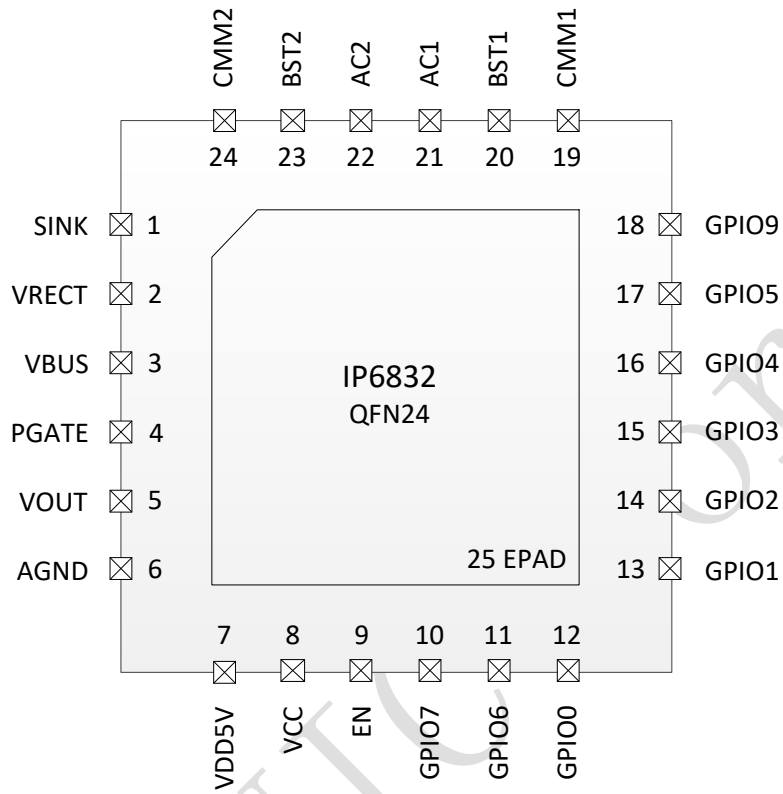


Figure 2 IP6832 Pin Definition

Pin Num	Name	I/O	Description
1	SINK	I	VRECT voltage clamping port.
2	VRECT	O	Synchronous rectification output filter port.
3	VBUS	I	Wired charging input port.
4	PGATE	O	Wired charging and wireless charging path switching driver output.
5	VOUT	O	Power LDO output port.
6	AGND	I	Analog ground.
7	VDD5V	O	5V power supply, connect to GND with 2.2uF capacitor.
8	VCC	O	3.3V power supply, connect to GND with 2.2uF capacitor.
9	EN	I	Enable port, effective at high level.
10	GPIO7	O	GPIO
11	GPIO6	O	GPIO
12	GPIO0	O	GPIO
13	GPIO1	O	GPIO
14	GPIO2	O	GPIO
15	GPIO3	O	GPIO
16	GPIO4	O	GPIO
17	GPIO5	O	GPIO
18	GPIO9	O	GPIO
19	CMM1	O	ASK modulation port, connect to AC1 with 10~22nF capacitor.
20	BST1	O	Bootstrap capacitors for driving the high side FETs of the synchronous rectifier. Connect to AC1 with 22nF capacitor.
21	AC1	I	AC input from receiver coil.
22	AC2	I	AC input from receiver coil.
23	BST2	O	Bootstrap capacitors for driving the high side FETs of the synchronous rectifier. Connect to AC2 with 22nF capacitor.
24	CMM2	O	ASK modulation port, connect to AC2 with 10~22nF capacitor.
25	GND	-	System and power ground.

## 7 System Diagram

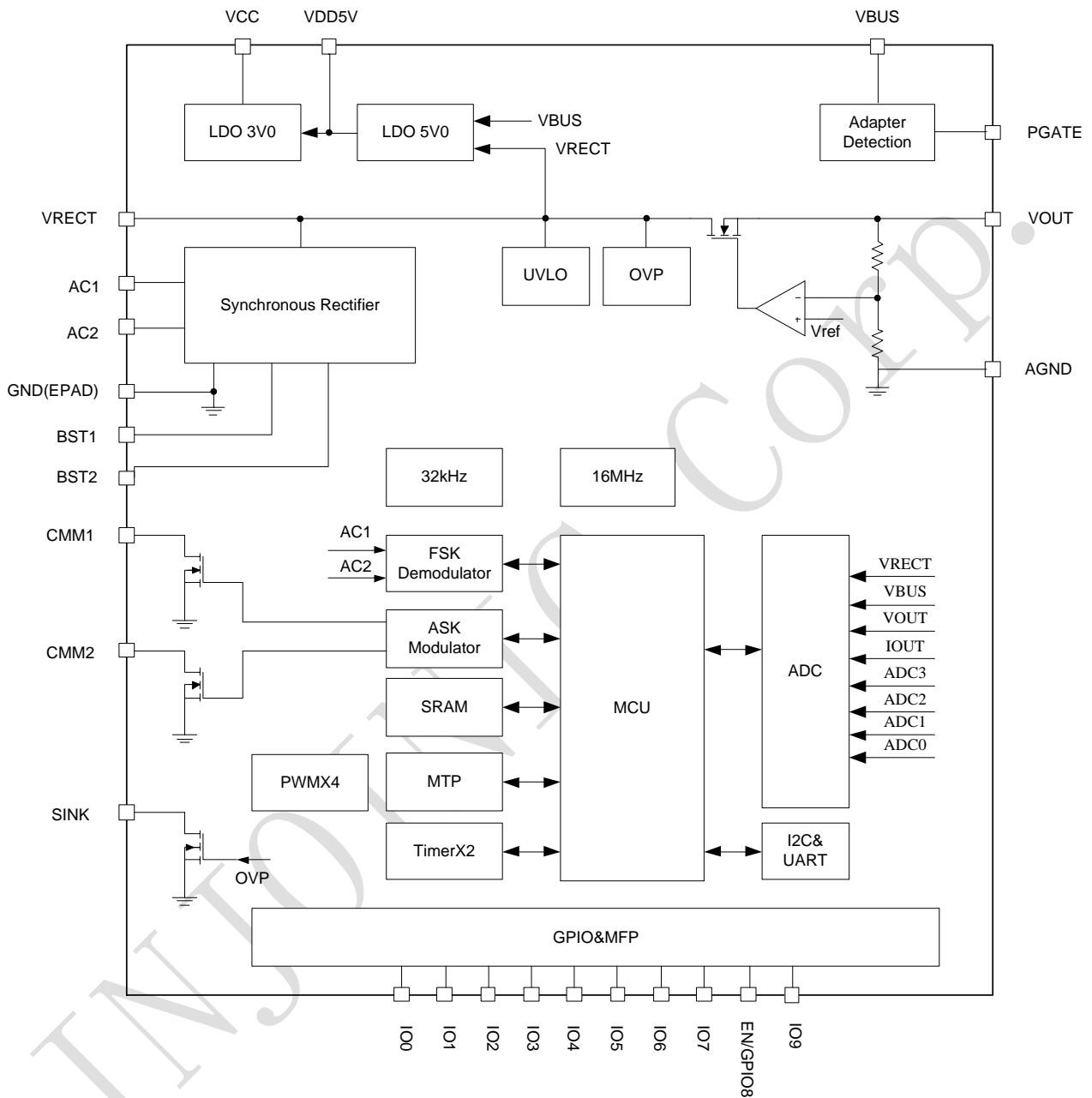


Figure 3 IP6832 Internal System Diagram

## 8 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)

Parameter	Symbol	Min	Max	Unit
Input Voltage Range	AC1/2	-0.3	20	V
	VBUS	-0.3	20	V
	SINK	-0.3	20	V
Output Voltage Range	VRECT	-0.3	20	V
	VOUT	-0.3	9	V
	VDD5V/VCC	-0.3	8	V
	PGATE	-0.3	20	V
	CMM1/2	-0.3	20	V
	BST1/2	-0.3	30	V
I/O Voltage Range	GPIO0-9,EN	-0.3	8	V
Storage Temperature Range	T <sub>stg</sub>	-55	150	°C
Thermal Resistance (Junction to Ambient)	$\theta_{JA}$	40		°C/W
ESD (Human Body Model)	ESD	4		KV

\*Stresses beyond these listed parameter may cause permanent damage to the device.

Exposure to Absolute Maximum Rated conditions for extended periods may affect device reliability.

## 9 Recommended Operating Conditions

Parameter	Symbol	Min	Type	Max	Unit
Rectified Output Voltage	VRECT	3	9	14	V
Load Current	I	0	1.2	1.5	A
VBUS Input Voltage	VBUS	4.5	-	9	V
Operating Temperature	T <sub>A</sub>	0	-	85	°C

\*Device performance cannot be guaranteed when working beyond these Recommended Operating Conditions.

## 10 Electrical Characteristics

Unless otherwise specified.  $T_A=0^{\circ}\text{C} \sim 85^{\circ}\text{C}$

Parameter	Symbol	Test conditions	Min	Type	Max	Unit
<b>VRECT</b>						
V <sub>RECT_UVLO</sub> Threshold	V <sub>RECT_UVLO</sub>	V <sub>RECT</sub> :5V->0V	2.8	2.9	3.0	V
V <sub>RECT_UVLO</sub> Threshold Hysteresis	V <sub>RECT_UVLO</sub> Hyteresis	V <sub>RECT</sub> : V <sub>RECT_UVLO</sub> ->5V		0.25		V
V <sub>RECT_OVP</sub> Threshold	V <sub>RECT_OVP</sub>	V <sub>RECT</sub> :5V->20V	14.5 16.5	15 17	15.5 17.5	V
V <sub>RECT_OVP</sub> Recover Threshold	V <sub>RECT_OVP</sub> Recover	V <sub>RECT</sub> : V <sub>RECT_OVP</sub> ->5V		12		V
<b>VBUS</b>						
V <sub>BUS</sub> Input Voltage	V <sub>BUS</sub>		4.5	5	9	V
V <sub>BUS_UVLO</sub> Threshold	V <sub>BUS_UVLO</sub>	V <sub>BUS</sub> :5V->0V	3.8	3.9	4.0	V
V <sub>BUS_UVLO</sub> Threshold Hysteresis	V <sub>BUS_UVLO</sub> Hyteresis	V <sub>BUS</sub> : V <sub>BUS_UVLO</sub> ->5V		0.3		V
V <sub>BUS_OVP</sub> Threshold	V <sub>BUS_OVP</sub>	V <sub>BUS</sub> :5V->20V		10.5		V
V <sub>BUS_OVP</sub> Threshold Hysteresis	V <sub>BUS_OVP</sub> Hyteresis	V <sub>BUS</sub> : V <sub>BUS_OVP</sub> ->5V		0.5		V
<b>LDO</b>						
LDO Output Voltage	V <sub>SET_LDO</sub>	V <sub>RECT</sub> > V <sub>out_ldo</sub>	3.6V~9V Programmable			V
LDO Voltage Regulation Step	V <sub>STEP_LDO</sub>		50			mV
LDO Input Dynamic Power Management	V <sub>DPM_LDO</sub>		3.9V~4.6V Programmable			V
LDO Output Current Limit	I <sub>LIMIT_LDO</sub>	Programmable			1600	mA
<b>Quiescent Current</b>						
V <sub>RECT</sub> Quiescent Current	I <sub>Q_VRECT</sub>	V <sub>RECT</sub> =5V,LDO is off		2	5	mA
V <sub>BUS</sub> Quiescent Current	I <sub>Q_VBUS</sub>	V <sub>BUS</sub> =5V only		2	5	mA
<b>System</b>						
VDD5V	VDD5V	2.2uF, I <sub>VDD5V</sub> =30mA	4.5	5	5.5	V
VCC	VCC	VDD5V		3.1		V
VCC Load Capacity	I <sub>VCC</sub>	VCC Maximum load current			50	mA
GPIO Logic High Level	V <sub>IH</sub>	GPIO0~9		0.7*VCC		V



GPIO Logic Low Level	$V_{IL}$	GPIO0~9		0.3*VCC		V
EN Wake-up Level	$V_{EN\_WAKE}$		1.5			V
Thermal Shut Down Temperature	$T_{OTP}$	Rising temperature	130	140	150	°C
Thermal Shut Down Hysteresis	$\Delta T_{OTP}$		30	40	50	°C

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## 11 Function Description

### 11.1 Synchronous Rectification

IP6832 integrates a high-efficiency full-bridge synchronous rectification module, which consists of a logic detection circuit, four N-MOSFETs and a driver circuit. Initially, AC current from the receiving coil flows through the parasitic diodes of the MOSFET, providing the chip with a start-up voltage. When the chip is powered on, the system switches the working mode of the rectifier bridge according to the load current. The rectifier bridge works in asynchronous mode (parasitic diode mode) at light load, and synchronous mode (MOSFET switch mode) at heavy load. The switching of working mode ensures high efficiency and stability of wireless charging.

### 11.2 Wireless Power Supply

IP6832 integrates wireless charging ASK modulation circuit and FSK demodulation circuit to realize two-way wireless charging communication and support private protocol development.

IP6832 integrates rectifier overvoltage protection circuit, when the rectifier voltage VRECT exceeds 15V (the gear can be configured by software), it will trigger the VRECT voltage clamping function to limit the VRECT voltage.

### 11.3 Wired Power Supply

IP6832 supports VRECT (wireless) and VBUS (wired) for power supply, and supports path switching between wired power supply and wireless charging.

### 11.4 Voltage Regulated LDO

Due to the position freedom of wireless charging, the rectifier voltage VRECT is not a stable voltage, and the rectifier voltage VRECT fluctuates greatly during the process of moving the charging equipment. IP6832 integrates a regulated LDO. The rectified voltage, VRECT, passes through the internal regulated LDO to provide a stable DC voltage to the downstream load. The output voltage and current of the regulated LDO can be set by software, and the voltage can be set in the range of 3.6V~9V in steps of 50mV; The output current limit setting range is 0~1600mA in steps of 50mA.

The regulated LDO has safety protection functions such as input undervoltage protection, input dynamic power management (DPM), output overcurrent protection, and output current limiting. When the charging device moves or deflects, the rectifier voltage VRECT will drop. When it falls below the DPM threshold of LDO, the regulated LDO will automatically reduce the output current, maintain the uninterrupted wireless charging, and improve the anti-deflection ability of wireless charging.

## 11.5 Low Power Mode and Wake Up

IP6832 supports deep sleep mode, and the power consumption in deep sleep mode is less than 2uA. In deep sleep mode, the IP6832 can be woken up by pulling the EN pin high by 50ms.

## 11.6 MCU

IP6832 integrates 32-bit MCU, and has rich peripheral resources such as Timer, PWM, ADC, I2C, UART, GPIO, etc., which is convenient for the customization of the whole product function without the need for external MCU.

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## 12 Typical Application Schematic

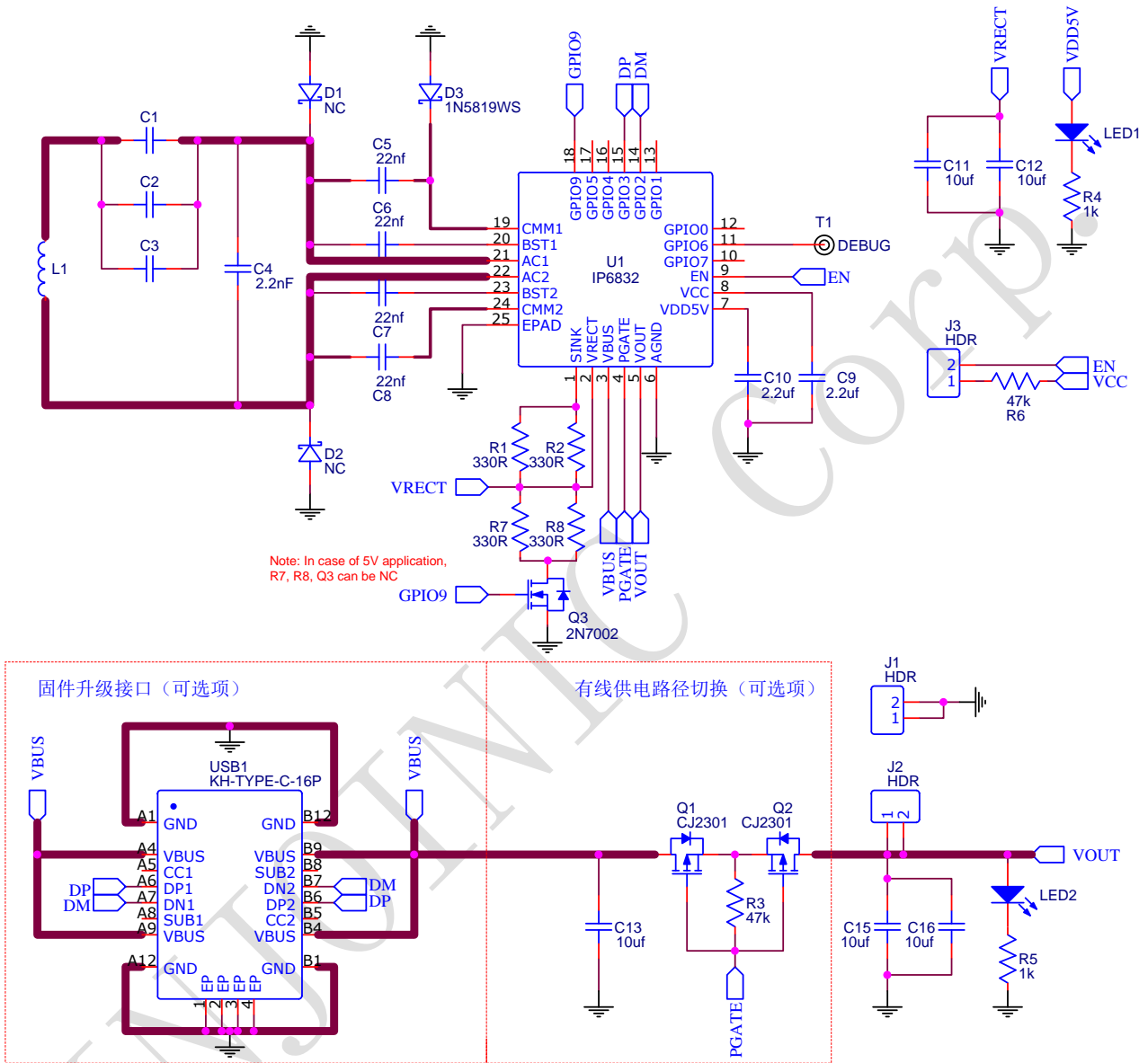
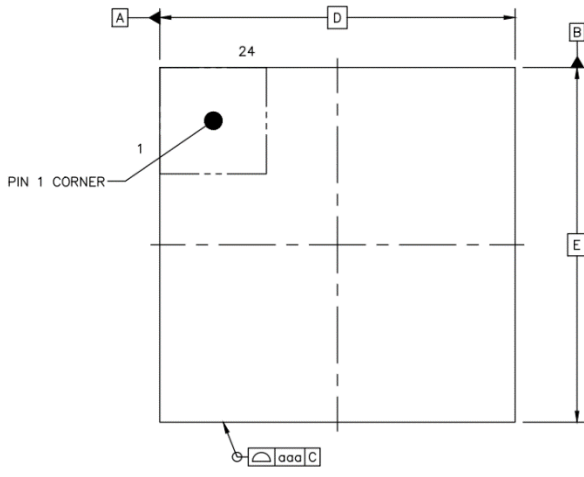


Figure 4 IP6832 Typical Application Schematic

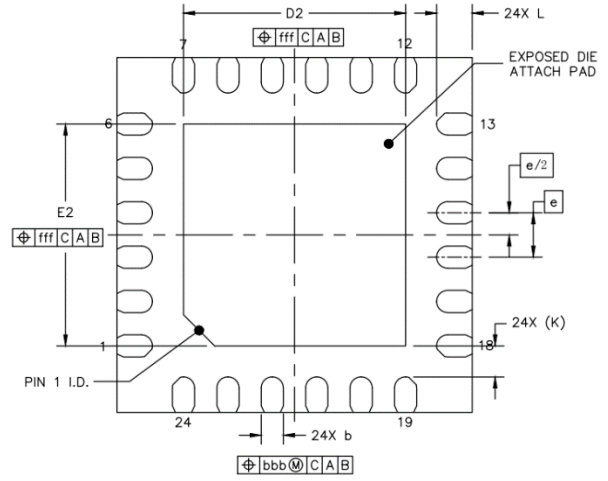
## 13 BOM

Num	Part Name	Position	Specification	Quantity
1	Resonant Capacitor	C1,C2,C3	C0603-10%-50V	3
2	Resonant Inductance	L1	Inductance parameters are selected according to the actual project	1
3	2.2nF	C4	C0603-10%-50V	1
4	22nf	C5,C6,C7,C8	C0603-10%-50V	4
5	2.2uf	C9,C10	C0603-10%-25V	2
6	10uf	C11,C12,C13,C15,C16	C0603-10%-25V	5
7	NC	D1,D2	SOD-123FL_L2.8-W1.8-LS3.8-RD	2
8	1N5819WS	D3	SOD-323_L1.8-W1.3-LS2.5-RD	1
9	HDR	J1,J2,J3	HDR-M-2.54_1X2	3
10	LED	LED1,LED2	LED0603_RED	2
11	CJ2301	Q1,Q2	SOT-23-3	2
12	2N7002	Q3	SOT-23-3	1
13	330R	R1,R2,R7,R8	R0805-5%-0.75W	4
14	47k	R3,R6	R0603-5%	2
15	1k	R4,R5	R0603-5%	2
16	TYPE-C-16P	USB1	USB-C-SMD_KH-TYPE-C-16P	1
17	IP6832	U1	QFN24-4mm*4mm	1

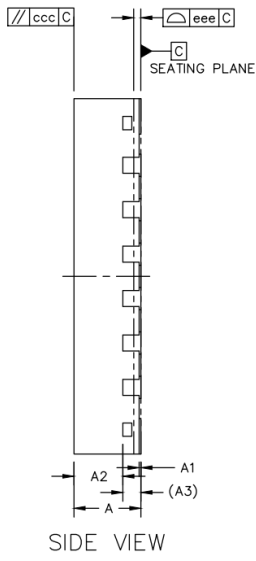
## 14 Package



TOP VIEW



BOTTOM VIEW



SIDE VIEW

UNIT : mm		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.7	0.75	0.8
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	---	0.55	---
L/F THICKNESS		A3	0.203 REF		
LEAD WIDTH		b	0.2	0.25	0.3
BODY SIZE	X	D	4 BSC		
	Y	E	4 BSC		
LEAD PITCH		e	0.5 BSC		
EP SIZE	X	D2	2.4	2.5	2.6
	Y	E2	2.4	2.5	2.6
LEAD LENGTH		L	0.35	0.4	0.45
LEAD TIP TO EXPOSED PAD EDGE		K	0.35 REF		
PACKAGE EDGE TOLERANCE		aaa	0.1		
MOLD FLATNESS		ccc	0.1		
COPLANARITY		eee	0.08		
LEAD OFFSET		bbb	0.1		
EXPOSED PAD OFFSET		fff	0.1		

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